**Checkpoint 3 Progress Report/Road Map**

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For this checkpoint we mainly focused on getting our advanced design features implemented. There were a few main advanced design features that we focused on. We primarily focused on making our RISC-V Processor two-issue superscalar. Also we worked on a multiplier extension as well as a bit manipulation extension. We also worked on making pipelined caches. We finished making a pipeline instruction cache which supports read, but as of writing this we still need to get our pipelined instruction cache finished. For now we’re using one of the provided caches for the data cache. We also are working on integrating bit manipulation and multiply extension into our processor as well. For superscalar we have a scoreboard done as well as multiple things parameterized. We are struggling a bit with superscalar at the moment but hope to really put our heads down over the next week going into checkpoint 4.

For the upcoming checkpoint we will mostly focus on testing and verifying as well as integrating our advanced design features. Our number one focus will be having at least a correct working processor for the design competition. Mostly because if we do not have a working processor then we cannot participate in the competition. However, this is just our baseline goal and hope to accomplish a lot more besides just that. Mesa will be focusing on finishing up the write aspect of the pipeline data cache. Victor will focus on the multiply extension. Suchir will mainly focus on the superscalar portion. However, being that superscalar is a much more daunting task than the other two aforementioned advanced design features. Mesa and Victor will pivot to helping Suchir with superscalar after finishing their respective tasks. We plan on using RVFI monitor in order to verify that our final design works and run it through all the checkpoint codes as well as the comp codes. We look forward to the competition :)

